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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,359	09/19/2003	Chi-Chun Chen	TS01-1488	8170

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EXAMINER	
SMITH, FRANCIS P	
ART UNIT	PAPER NUMBER
4151	
MAIL DATE	DELIVERY MODE
01/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/666,359	CHEN ET AL.	
	Examiner	Art Unit	
	FRANCIS P. SMITH	4151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/2003; 2/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Page 4, first paragraph of the specification is incomplete. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4-15, 20-24, 26-37, 42, and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Raaijmakers et al. (US 6,348,420).

For claims 1 and 23, Raaijmakers teaches processes for forming ultra thin dielectric stacks of high quality. First, a wafer is cleaned to provide a clean silicon surface (i.e. providing a silicon substrate) col. 13, lines 43-45. Then, the method includes loading the said substrate into a processing chamber at 780°C where a first oxide layer grows on the semiconductor structure (i.e. thermal oxide layer) col. 13, lines 57-59. A silicon nitride layer is then deposited over the thermal oxide layer forming a stacked gate dielectric (col. 3, lines 20-35). During an anneal step, the substrate is exposed to a nitriding agent (i.e. nitridation process) followed by exposure to an oxidizing agent (i.e. reoxidation process) col. 15, lines 21-37. A remote plasma generator is located upstream from the reaction chamber and is connected to each gas

line via separate mass flow controller and valves, allowing for said plasma nitridation/reoxidation processes (col. 7, lines 44-65).

Regarding claims 2 and 24, Raaijmakers teaches a processes where the thermal oxide layer grows to about 0.5 nm (or 5 angstroms) while the silicon nitride layer grows to about 3 nm (or 30 angstroms) col. 14, lines 3-5, 19-21.

For claims 4-7 and 26-29, Raaijmakers teaches a processes for forming ultra thin dielectric stacks of high quality where the dielectric growth and deposition steps (i.e. formation of the thermal silicon oxide and nitride layers) are conducted in the rage of 650-850°C (col. 11, lines 7-23).

As per claims 8 -10 and 30-32, Raaijmakers teaches a process for forming ultra thin dielectric stacks of high quality where oxide layer is a thermal silicon oxynitride and the CVD nitride layer consists of silicon nitride (col. 11, lines 25-29; col. 14, lines 1-5,18-21).

Regarding claims 11 and 33, Raaijmakers teaches a method of forming a nitride layer by a remote plasma enhanced (RPECVD) process. (col. 18, lines 34-46).

For claims 12-15 and 34-37, Raajimakers discloses a process for forming ultra thin dielectric stacks of high quality where the plasma nitridation process is conducted at a temperature range of 650-680°C in a reaction chamber set within a range of 1-80 torr (col. 20, lines 34-36; col. 19, lines 22-26)

As for claims 20,21,42, and 43, Raaijmakers teaches a process for forming ultra thin dielectric stacks of high quality aided by plasma energy with an optional anneal step using nitriding or oxidizing agents (i.e. reoxidation step). The oxidant my be N_2O, NO,

or O_2 (col. 11, lines 38-52; col. 17, lines 66-67; col. 20, lines 64-67).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raaijmakers et al. (US 6,348,420) in view of Bloom et al. (US 6,228,779).

For claims 3 and 25, Raaijmakers teaches processes for forming ultra thin dielectric stacks of high quality. A thermal oxide layer grows to about 0.5 nm (or 5 angstroms) while the silicon nitride layer is about 3 nm (or 30 angstroms) col. 14, lines 3-5, 19-21. Raaijmakers, however is silent regarding a nitride layer of 5-15 angstroms.

Bloom teaches a method of forming a dense and stable dielectric layer of silicon nitride and silicon dioxide for use in transistors of ULSI circuits where the nitride layer is placed above the silicon dioxide layer. The said silicon nitride layer may be in a range of 5-20 angstroms (col. 3, lines 15-16). It would be obvious to one skilled in the art at the time of the invention to modify Raaijmakers' method by incorporating Bloom's nitride layer thickness in order to find the optimum nitride layer thickness for preventing the migration of dopants such boron into the silicon dioxide dielectric layer.

8. Claims 16-19 and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raaijmakers et al. (US 6,348,420).

Regarding claims 16-19 and 38-41, Raaijmakers teaches a process for forming ultra thin dielectric stacks of high quality aided by plasma energy with an optional anneal step using nitriding or oxidizing agents (i.e. reoxidation step). The oxidant my be comprised of N_2O, NO, or O_2 (col. 11, lines 38-52; col. 17, lines 66-67; col. 20, lines 64-67). For deposition processes, the wafer is preferably kept at a temperature below about 750°C in a chamber with a pressure range of 1-80 torr (col. 19, lines 22-26; col. 20, lines 19-21).

Although Raaijmakers states that the processing steps conducted in situ are conducted under similar or identical temperatures and pressures (col. 19, lines 18-22,) Raaijmakers is silent with regard to a specific temperature and pressure range during the reoxidation step. However, It would be obvious to one skilled in the art at the time of the invention to maintain the parameters of the reactor chamber at the temperature and pressure of the silicon oxynitride and nitride deposition during the annealing (reoxidation) step in order to avoid pressure/temperature ramping and minimize thermal stress that could cause peeling of coatings from the substrate.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-3 and 22-25 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3 and 8-10 of Chen et al. U.S. Patent No. 6,642,117. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Regarding claims 1 and 23, Chen '117 teaches a method for forming composite dielectric layers where a (oxidizable) substrate is first provided and a thermal oxide layer is formed upon said substrate. Then, a nitride layer is deposited on the oxide layer to form an initial stacked gate dielectric. The initial stacked gate dielectric is then subject to annealing in a nitriding atmosphere (e.g. a plasma nitridation process). This nitrided composite stack layer is then annealed in an oxidizing atmosphere, which is analogous to a plasma reoxidation process (claims 1 and 8).

As for claims 2, 3, 24, and 25, Chen '117 discloses a thermal oxide layer formed to a thickness of about 5-15 angstroms and a deposited nitride layer formed to a thickness of about 5-30 angstroms (claims 3 and 10).

For claim 22, Chen '117 teaches the use of an oxidizable substrate consisting of semiconductor materials such as silicon (claims 2 and 9).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRANCIS P. SMITH whose telephone number is (571)270-3717. The examiner can normally be reached on Monday through Friday 7:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mikhail Kornakov can be reached on (571)272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FPS

/Michael Kornakov/
Supervisory Patent Examiner, Art Unit 4151